2K x 8
2048 x 8-BIT STATIC RAM

- **Fully Static Operation; No Clocks, Refresh or Latches**
- **EPROM Compatible Pinout**
- **Industry Standard 24-Pin Package**
- **Two Line Control, $\overline{CE}$ Controls Power-Down, $\overline{OE}$ Controls Output Buffers — Eliminates Bus Contention**
- **150 ns Maximum Access Time**
- **Auto Power-Down**

The Intel® 2K x 8 is a 16,384-bit static RAM organized as 2048 words by 8 bits. It employs fully static circuitry which eliminates the need for clocks, refresh, or address setup and hold times. The auto power-down feature cuts power consumption when the device is disabled.

The 24-pin industry standard pinout allows easy upgrades to 4K x 8 static RAMs and compatibility to the 2732 4K x 8 and 2764 8K x 8 EPROMs in 28-pin sites. The two line control simplifies decoding and eliminates any possibility of bus contention.

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	OUTPUT	POWER
H	X	X	NOT SELECT	HIGH Z	STANDBY
L	H	H	SELECTED	HIGH Z	ACTIVE
L	H	L	READ	ACTIVE	ACTIVE
L	L	X	WRITE	HIGH Z	ACTIVE

PIN NAMES

A_0—A_{10}	ADDRESS INPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
D_0—D_7	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)
GND	GROUND

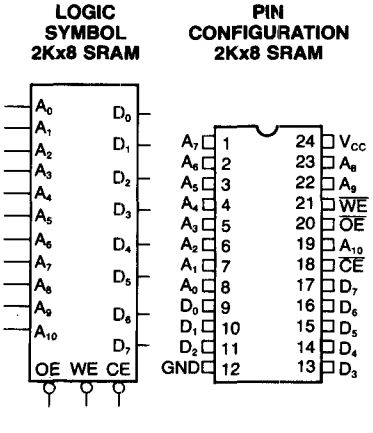


Figure 1. 2K x 8 Pin Diagram

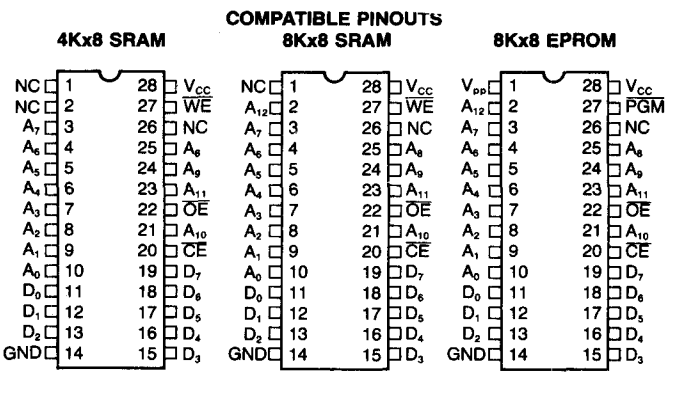


Figure 2. Compatible Pinouts

4K x 8
4096 x 8-BIT STATIC RAM

- **Fully Static Operation; No Clocks, Refresh or Latches**
- **EPROM Compatible JEDEC Standard Pinout**
- **2764 Compatible 28-Pin Package — Allows Easy Upgrade To 8K x 8 SRAM Without Jumpers**
- **Two Line Control, $\overline{CE}$ Controls Power-Down, $\overline{OE}$ Controls Output Buffers — Eliminates Bus Contention**
- **150 ns Maximum Access Time**
- **Auto Power-Down**

The Intel® 4K x 8 is a 32,768-bit static RAM organized as 4096 words by 8 bits. It employs fully static circuitry which eliminates the need for clocks, refresh, or address setup and hold times. The auto power-down feature cuts power consumption when the device is disabled.

The 28-pin JEDEC standard pinout allows easy upgrades to 8K x 8 static RAMs and compatibility to the 2732 4K x 8 and 2764 8K x 8 EPROMs — without jumpers. The two line control simplifies decoding and eliminates any possibility of bus contention.

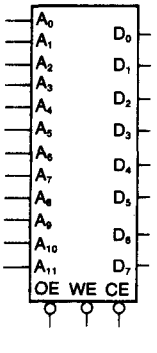
TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	OUTPUT	POWER
H	X	X	NOT SELECT	HIGH Z	STANDBY
L	H	H	SELECTED	HIGH Z	ACTIVE
L	H	L	READ	ACTIVE	ACTIVE
L	L	X	WRITE	HIGH Z	ACTIVE

PIN NAMES

A_0—A_{11}	ADDRESS INPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
D_0—D_7	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)
GND	GROUND

LOGIC SYMBOL 4K x 8



PIN CONFIGURATION 4Kx8 SRAM

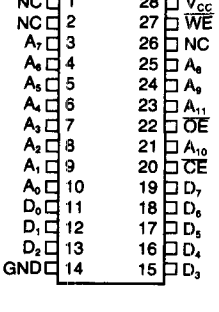
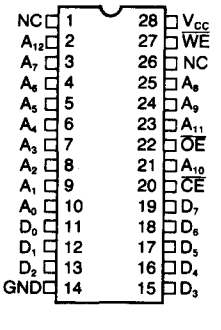


Figure 1. 4K x 8-Pin Diagram

COMPATIBLE PINOUTS

8Kx8 SRAM



8Kx8 EPROM

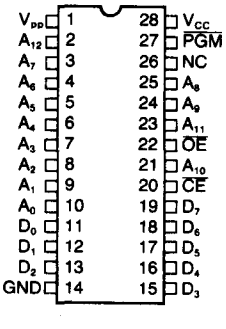


Figure 2. Compatible Pinouts

2764
(8K x 8) UV ERASABLE PROM

- **200 ns (2764-2) Maximum Access Time . . . HMOS*-E Technology**
- **Compatible to High Speed 8mHz 8086-2 MPU . . . Zero WAIT State**
- **Two Line Control**
- **Pin Compatible to 2732A EPROM**
- **Industry Standard Pinout . . . JEDEC Approved**
- **Low Active Current...100mA Max.**

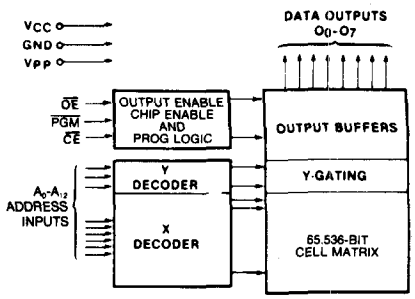
The Intel® 2764 is a 5V only, 65,536-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The standard 2764 access time is 250ns with speed selection available at 200ns. The access time is compatible to high performance microprocessors, such as Intel's 8mHz 8086-2. In these systems, the 2764 allows the microprocessor to operate without the addition of WAIT states.

An important 2764 feature is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

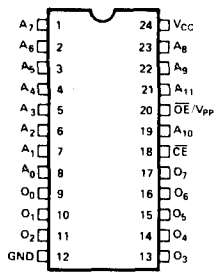
The 2764 has a standby mode which reduces the power dissipation without increasing access time. The active current is 150mA while the standby current is only 50mA. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

The 2764 is fabricated with HMOS*-E technology, Intel's high-speed N-channel MOS Silicon Gate Technology.

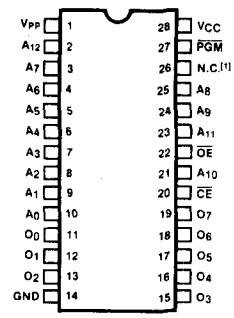
BLOCK DIAGRAM



2732A PIN CONFIGURATION



2764 PIN CONFIGURATION



[1] For total compatibility and upgradability from the 2732A and ROMs provide a trace to pin 26.

MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	x	x	V_{CC}	V_{CC}	High Z
Program	V_{IL}	x	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	x	x	V_{PP}	V_{CC}	High Z

x can be either V_{IL} or V_{IH}

PIN NAMES

A_0-A_{12}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO CONNECT

*HMOS is a patented process of Intel Corporation.

PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....−10°C to +80°C
Storage Temperature .....−65°C to +125°C
All Input or Output Voltages with
Respect to Ground .....+6V to −0.6V
V_{PP} Supply Voltage with Respect to Ground
During Programming .....+22V to −0.6V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Conditions During Read

	2764	2764-2	2764-3	2764-4
Operating Temperature Range	0°C–70°C	0°C–70°C	0°C–70°C	0°C–70°C
V_{CC} Power Supply[1,2]	5V± 5%	5V ± 5%	5V ± 5%	5V ±5%
V_{PP} Voltage[2]	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

READ OPERATION

D.C. AND OPERATING CHARACTERISTICS

Symbol	Parameter	Limits			Unit	Conditions
		Min	Typ[3]	Max		
I_{LI}	Input Load Current			10	μA	$V_{IN} = 5.25V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.25V$
I_{PP1}[2]	V_{PP} Current Read			15	mA	$V_{PP} = 5.25V$
I_{CC1}[2]	V_{CC} Current Standby			50	mA	$\overline{CE} = V_{IH}$
I_{CC2}[2]	V_{CC} Current Active		70	150	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	−.1		+.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

NOTES: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.

A.C. CHARACTERISTICS

Symbol	Parameter	2764-2 Limits		2764 Limits		2764-3 Limits		2764-4 Limits		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		200		250		300		450	ns	$\overline{CE}=\overline{OE}=V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300		450	ns	$\overline{OE}=V_{IL}$
t_{OE}	Output Enable to Output Delay	10	70	10	100	10	150	10	150	ns	$\overline{CE}=V_{IL}$
t_{DF}	Output Enable High to Output Float	0	60	0	90	0	130	0	130	ns	$\overline{CE}=V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		ns	$\overline{CE}=\overline{OE}=V_{IL}$

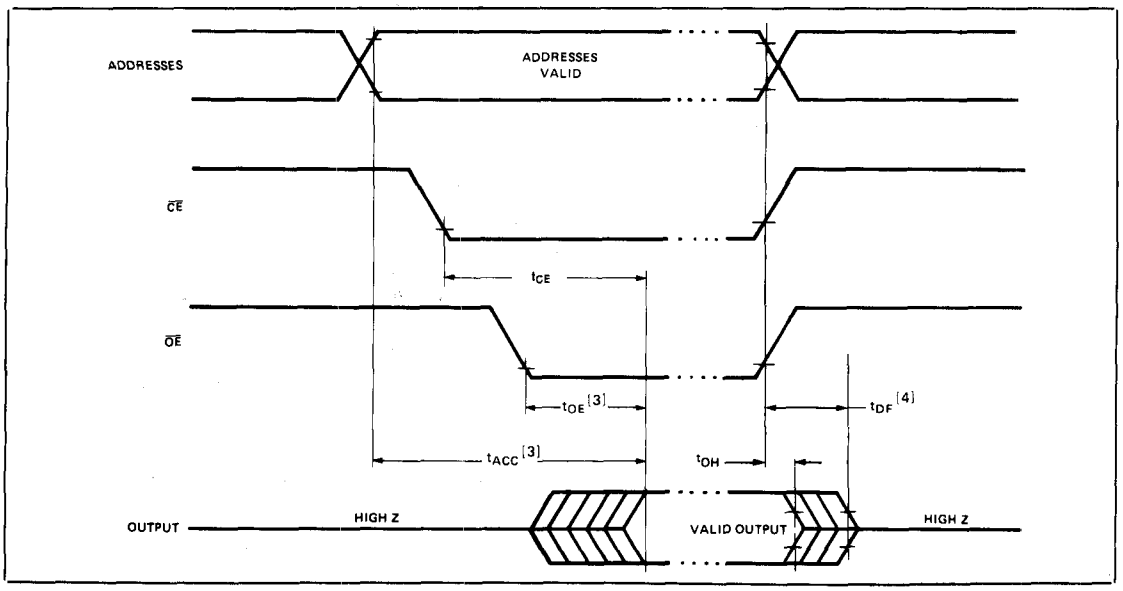
CAPACITANCE [1] $T_A = 25°C$, f = 1MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN}=0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT}=0V$

A.C. TEST CONDITIONS

Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. WAVEFORMS



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

ERASURE CHARACTERISTICS

The erasure characteristics of the 2764 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2764 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2764 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2764 window to prevent unintentional erasure.

The recommended erasure procedure for the 2764 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The 2764 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2764 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

TABLE 1. MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	x	x	V_{CC}	V_{CC}	High Z
Program	V_{IL}	x	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	x	x	V_{PP}	V_{CC}	High Z

x can be either V_{IL} or V_{IH}

READ MODE

The 2764 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The 2764 has a standby mode which reduces the active power current from 150mA to 50mA. The 2764 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connection. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING (See Programming Instruction Section for Waveforms.)
Programming is the same as Intel's 2732A except that $\overline{OE}/V_{PP}$ is not multiplexed. They have separate pins. Like the 2732A, ***exceeding 21.5V will damage the 2764.***

Initially, and after each erasure, all bits of the 2764 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2764 is in the programming mode when V_{PP} input is at 21V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 21V. When the address and data are stable, a 50 msec, active low, TTL program pulse is applied to $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec.

Programming of multiple 2764s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2764s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled 2764s.

Program Inhibit

Programming of multiple 2764s in parallel with different data is also easily accomplished. A high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other 2764s from being programmed. Except for $\overline{CE}$ (or $\overline{PGM}$), all like inputs (including $\overline{OE}$) of the parallel 2764s may be common. A TTL low level pulse applied to a 2764 $\overline{CE}$ and $\overline{PGM}$ input with V_{PP} at 21V will program that 2764.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{CE}$ and $\overline{OE}$ at V_{IL}. However, $\overline{PGM}$ is at V_{IH}.